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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,519	11/17/2003	Simon Charles Watt	550-480	6837
23117 7590 11/14/2008 NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203				
EXAMINER				
ABEDIN, SHANTO				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/714,519

Applicant(s)

WATT ET AL.

Examiner

SHANTO M. ABEDIN

Art Unit

2436

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 August 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 2, 4-11, 13-25, 27-34 and 36-47 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-2, 4-7, 11, 13, 17, 20-25, 27-30, 34, 36, 40 and 43-47 is/are rejected.
- 7) ☒ Claim(s) 8-10, 14-15, 16, 18, 19, 31-33, 37-39 and 41-42 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-946)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 08/14/2008
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. This is in response to the communication filed on 08/14/2008.
2. Claims 1-2, 4- 11, 13-25, 27-34 and 36-47 are currently presented for the examination.
3. Claims 8-10, 14-15, 16, 18, 19, 31-33, 37-39 and 41-42 are objected.
4. Claims 1-2, 4-7, 11, 13, 17, 20-25, 27-30, 34, 36, 40 and 43-47 have been rejected.

Response to Arguments

5. The applicant's arguments regarding previous 35 USC 103(a) type rejections are fully considered, however, moot in view of the new grounds of rejection presented in this office action.
6. The applicant's arguments regarding previous obviousness type double patenting rejections are fully considered, and found persuasive. The previous obviousness type double patenting rejections are withdrawn because of the terminal disclaimer approved on 09/08/2008.
7. The applicant's arguments regarding the previous 35 USC 101 type rejections are fully considered, and found not persuasive. However, the previous 35 USC 101 type rejections are withdrawn because of the amendments made to the claim 47.

Claim Objections

8. Claims 47 is objected because of the following informalities:

Regarding claim 47, it is objected under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. In particular, claim 47 is directed to a "computer program product",

however, the independent claim 24 (on which the claim 47 is dependent on) is directed to a method. Therefore, claim 47 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of the method in claim 24.

Claim 47 is further objected to because languages of the amended raise an issue regarding "new matter" situation. In particular, limitations such as "computer program product comprising a computer readable storage medium containing, computer readable instructions" were not found in the specification or originally filed claim set. The applicant is respectfully suggested to rewrite the claim in such a way so that a computer program product is used to 'store' computer readable instructions instead of using the phrase 'having', or introducing a "computer readable storage medium".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 17 and 40 are rejected under 35 USC 112 second paragraph for lacking antecedent basis for the claimed limitations. Claims 17 and 40 recite the limitation "said monitor mode", however, there is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 1-2, 4- 7, 11, 13, 20-25, 27-30, 34, 36, and 43-47 are rejected under 35 USC 103 (a) as being unpatentable over Christie et al (US 7165135 B1) in view of Knight (US 2003/0126520 A1) further in view of Kim et al (US 2003/0031235 A1)

Regarding claims 1 and 24, Christie et al discloses apparatus/ method for processing data, said apparatus/ method comprising:

a processor operable in a plurality of modes and a plurality of domains, said plurality of domains comprising a secure domain and a non-secure domain (Fig 1; related modes and domains; Col 4, starting at line 7, plurality of memory location associated with the plurality of the execution modes) said plurality of modes including:

at least one secure mode being a mode in said secure domain (Fig 1; secure modes and domains; Col 4, starting at line 7, plurality of memory location associated with the plurality of the execution modes) ; and

at least one non-secure mode being a mode in said non-secure domain (Fig 1; related modes and domains; Col 4, starting at line 7, normal mode and domain); wherein when said processor is executing a program in a secure mode said program has access to secure data which is not accessible when said processor is operating in a non-secure mode (Fig 1; Col 4, starting at line 65; Col 9, starting at line 62; Claim 1)

said processor is responsive to one or more exception conditions for triggering exception processing using an exception handler, said processor being operable to select said exception handler from among a plurality of possible exception handlers in dependence upon whether said processor is operating in said secure domain or said non-secure domain (Fig 1; Col 4, starting at line 7; Col 9, starting at line 62; Claim 1-9; exception/ interrupt handler based on whether processor/ system is operating in secure/ protected mode, or insecure/ normal modes); and control triggering of either a non-secure exception handler operating in a non-secure mode or a secure exception handler operating in a secure mode with any change of domain also being triggered when required (Fig 3; Col 4, line 29-67; Col 9, line 62- Col 10, line 67; Claims 1-9; controller , or mode capable processor to control exception handling based on modes/ domains)

Christie et al fails to disclose exception handlers in dependence upon an exception vector value associated with said exception condition and stored within an active exception vector table; and wherein said active exception vector table is one of a plurality of exception vector tables; and programmable configurations associated therewith.

However, Knight discloses exception handlers in dependence upon an exception vector value associated with said exception condition and stored within an active exception vector table; and wherein said active exception vector table is one of a plurality of exception vector tables (Par 0007, 0015-0019; Claims 1-24; exception vector table for exception, and exceptions having corresponding operational modes such as normal, protected/ private, and IRQ modes).

Furthermore, Kim et al discloses programmable configurations associated therewith that control triggering of either a non-secure exception handler operating in a non-secure mode or a secure exception handler operating in a secure mode with any change of domain also being triggered when

required (Par 021, 022, 055, 073, Claims 1 and 10; programmable configuration data/ memory for selection and switching between different modes)

Kim et al , Knight and Christie et al are analogous art because they are from the same field of endeavor of secure exception handling involving different operational/ execution modes. At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the teachings of Kim et al and Knight with Christie et al to design a method further including exception vector table and programmable configuration data in order to provide an alternative and efficient exception handling mechanism in a firmware or programmable device.

Regarding claim 2, Christie et al discloses apparatus wherein at least one of said exceptions is a selectable exception handled by a selectable one of either a non-secure exception handler operating in a non-secure mode or a secure exception handler operating in a secure mode; and at least one of said exceptions is a dedicated secure exception that is handled by a secure exception handler operating in a secure mode (Col 9, starting at line 45; Claim 2; exception handling logic).

Furthermore, Knight discloses apparatus wherein at least one of said exceptions is a selectable exception handled by a selectable one of either a non-secure exception handler operating in a non-secure mode or a secure exception handler operating in a secure mode; and at least one of said exceptions is a dedicated secure exception that is handled by a secure exception handler operating in a secure mode (Par 0007, 0015-0019; Claims 1-24; processor for exception handling where each exceptions has corresponding different operational modes such as normal or protected modes; and exception handling depend on mode of operations)

Regarding claim 4, Christie et al discloses apparatus having a secure exception is triggered by one of a signal on a dedicated secure exception signal input and a non secure exception signal input (Col 9, starting at line 45; Claim 1-9).

Regarding claim 5, Christie et al discloses apparatus having an exception signal input shared between secure and non-secure exceptions and a further input signal cooperating with said exception signal input to control whether a secure exception handler or a non-secure exception handler is triggered (Col 9, starting at line 45; Claim 1-9).

Furthermore, **Knight** discloses exception signal input shared between secure and non-secure exceptions and a further input signal cooperating with said exception signal input to control whether a secure exception handler or a non-secure exception handler is triggered (Par 0007, 0015-0019; Claims 1-24; processor for exception handling where each exceptions has corresponding different operational modes such as normal or protected modes)

Regarding claim 6, Christie et al discloses apparatus wherein said secure exception handler is part of secure operating system operable in said secure mode (Col 9, starting at line 45; Claim 1-9).

Regarding claim 7, Christie et al discloses apparatus wherein said non-secure exception handler is part of a non-secure operating system operable in said non-secure mode (Col 9, starting at line 45; Claim 1-9).

Regarding claims 11 and 34, Christie et al fails to disclose wherein said exception conditions includes one of more of: a secure interrupt signal exception; a mode switching software interrupt signal; a reset exception; an interrupt signal exception; a software interrupt signal; an undefined instruction exception; a prefetch abort exception; a data abort exception; and a fast interrupt signal exception.

However, Knight discloses wherein said exception conditions includes one of more of: a secure interrupt signal exception; a mode switching software interrupt signal; a reset exception; an interrupt signal exception; a software interrupt signal; an undefined instruction exception; a pre fetch abort exception; a data abort exception; and a fast interrupt signal exception (Par 0011 to 0017).

Regarding claim 13, Christie et al discloses apparatus wherein said plurality of exception vector tables include a secure exception vector table selectable in said secure mode and a non-secure exception vector table selectable in said non-secure mode (Col 9, starting at line 45; interrupt vectors; Col 9, starting at line 45; exception handling logic).

Regarding claims 20 and 42-43, Christie et al discloses exception trap mask register is non-writable when said processor is not in non-secure domain (Col 3, starting at line 15; Claims 5-9; debug traps).

Regarding claims 21-23, 25, 27-30, 34, 36 and 44-47, they recite the similar limitations that already addressed rejecting claims 1-10, 12-18 and 24, therefore, claims 21-23,25-33, 35-41 and 44-47 are rejected applying as above rejecting claims 1-10,12-18, 24.

11. Claims 1 and 24 are further rejected under 35 USC 103 (a) as being unpatentable over Christie et al (US 7165135 B1) in view of Dahan et al (US 7237081 B2) further in view of Kim et al (US 2003/0031235 A1)

Regarding claims 1 and 24, Christie et al discloses apparatus/ method for processing data, said apparatus/ method comprising:

a processor operable in a plurality of modes and a plurality of domains, said plurality of domains comprising a secure domain and a non-secure domain (Fig 1; related modes and domains; Col 4, starting at line 7, plurality of memory location associated with the plurality of the execution modes) said plurality of modes including:

at least one secure mode being a mode in said secure domain (Fig 1; secure modes and domains; Col 4, starting at line 7, plurality of memory location associated with the plurality of the execution modes) ; and

at least one non-secure mode being a mode in said non-secure domain (Fig 1; related modes and domains; Col 4, starting at line 7, normal mode and domain); wherein when said processor is executing a program in a secure mode said program has access to secure data which is not accessible when said processor is operating in a non-secure mode (Fig 1; Col 4, starting at line 65; Col 9, starting at line 62; Claim 1)

said processor is responsive to one or more exception conditions for triggering exception processing using an exception handler, said processor being operable to select said exception handler from among a plurality of possible exception handlers in dependence upon whether said processor is operating in said secure domain or said non-secure domain (Fig 1; Col 4, starting at line 7; Col 9, starting at line 62; Claim 1-9; exception/ interrupt handler based on whether processor/ system is

operating in secure/ protected mode, or insecure/ normal modes); and programmable configurations associated therewith that control triggering of either a non-secure exception handler operating in a non-secure mode or a secure exception handler operating in a secure mode with any change of domain also being triggered when required (Fig 3; Col 4, line 29-67; Col 9, line 62- Col 10, line 67; Claims 1-9; controller , or mode capable processor to control exception handling based on modes/ domains)

Christie et al fails to disclose exception handlers in dependence upon an exception vector value associated with said exception condition and stored within an active exception vector table; and wherein said active exception vector table is one of a plurality of exception vector tables; and use of programmable configurations associated therewith.

However, Dahan et al discloses exception handlers in dependence upon an exception vector value associated with said exception condition and stored within an active exception vector table; and wherein said active exception vector table is one of a plurality of exception vector tables (Col 14, line 38- Col 19, line 65; specially Col 18, starts at line 46; exception/ interrupts vector table).

Dahan et al further discloses one or more exception conditions have respective programmable configurations associated therewith that control triggering of either a non-secure exception handler operating in a non-secure mode or a secure exception handler operating in a secure mode with any change of domain also being triggered when required (Col 16, line 1- Col 20, line 35; normal/ non-secure, and secure modes exceptions/ interrupts; SSM monitoring interrupts/ exceptions).

Furthermore, Kim et al discloses programmable configurations associated therewith that control triggering of either a non-secure exception handler operating in a non-secure mode or a secure exception handler operating in a secure mode with any change of domain also being triggered when

required (Par 021, 022, 055, 073, Claims 1 and 10; programmable configuration data/ memory for selection and switching between different modes)

Kim et al , Dahan et al and Christie et al are analogous art because they are from the same field of endeavor of secure exception handling involving different operational/ execution modes. At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the teachings of Kim et al , Dahan et al with Christie et al to design a method further including exception vector table in order to provide an alternative and efficient exception handling mechanism for a programmable or firmware type device.

Allowable Subject Matter

12. Claims 8-10, 14-15, 16, 18, 19, 31-33, 37-39 and 41-42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. Claims 17 and 40 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

14. Examiner's note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may be applied as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Finally, for any future amendments to claims, the applicant is respectfully suggested to incorporate the paragraph numbers from the specification upon which the support for such amendments were dependent on.

15. A shortened statutory period for response to this action is set to expire in 3 (Three) months and 0 (Zero) days from the mailing date of this letter. Failure to respond within the period for response will result in ABANDONMENT of the application (see 35 U.S.C 133, M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shanto M Z Abedin whose telephone number is 571-272-3551. The examiner can normally be reached on M-F from 9:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Moazzami Nasser, can be reached on 571-272-4195. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shanto M Z Abedin

Examiner, AU 2436

/Nasser G Moazzami/

Supervisory Patent Examiner, Art Unit 2436

